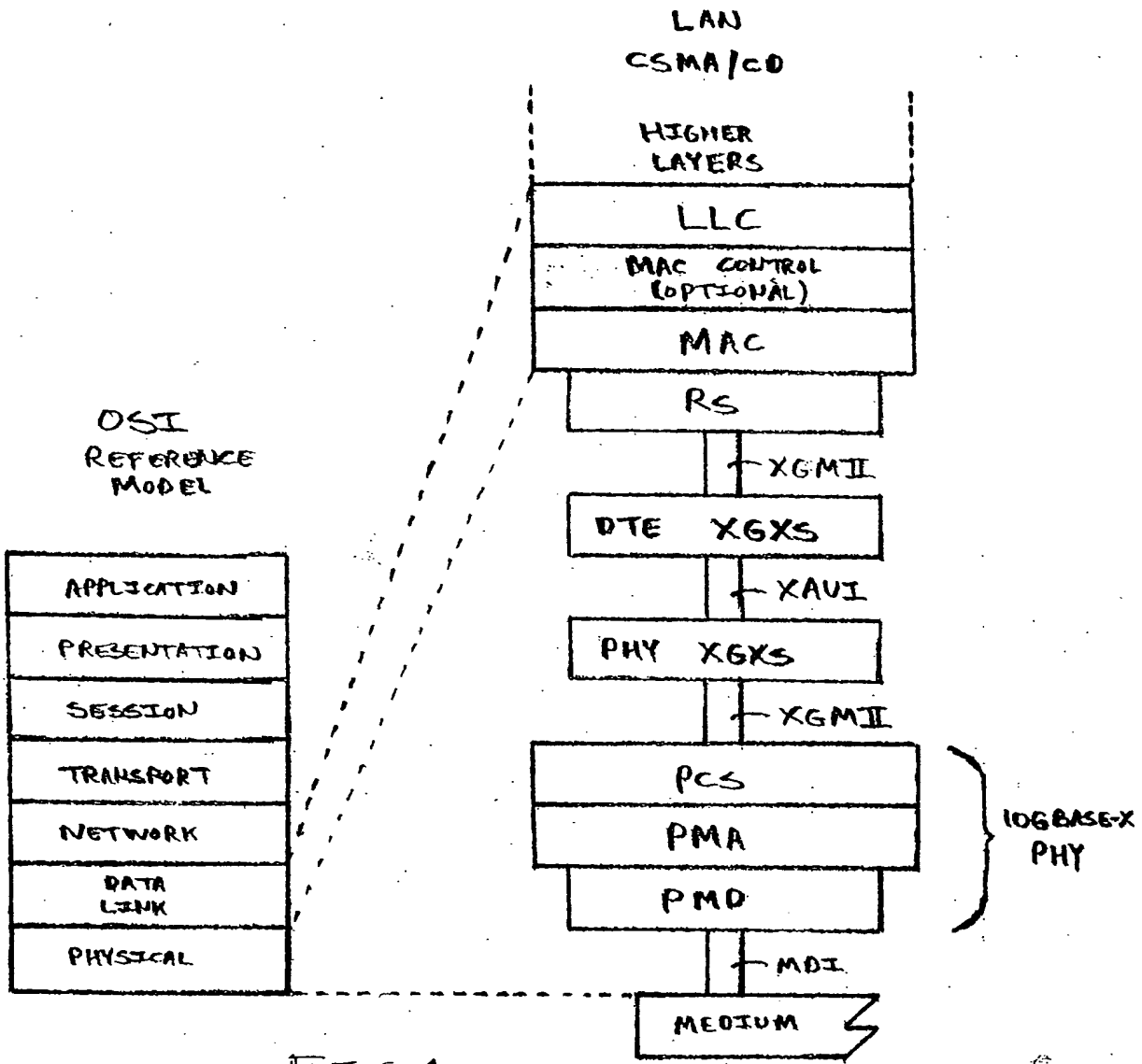

LAN
CSMA/CD
HIGHER LAYERS
LLC
MAC CONTROL (OPTIONAL)
MAC
RS
XGMII
DTE XGXS
XAUI
PHY XGXS
XGMII
PCS
PMA
PMD
10GBASE-X PHY
MDI
MEDIUM
OSI REFERENCE MODEL
APPLICATION
PRESENTATION
SESSION
TRANSPORT
NETWORK
DATA LINK
PHYSICAL

FIG.1

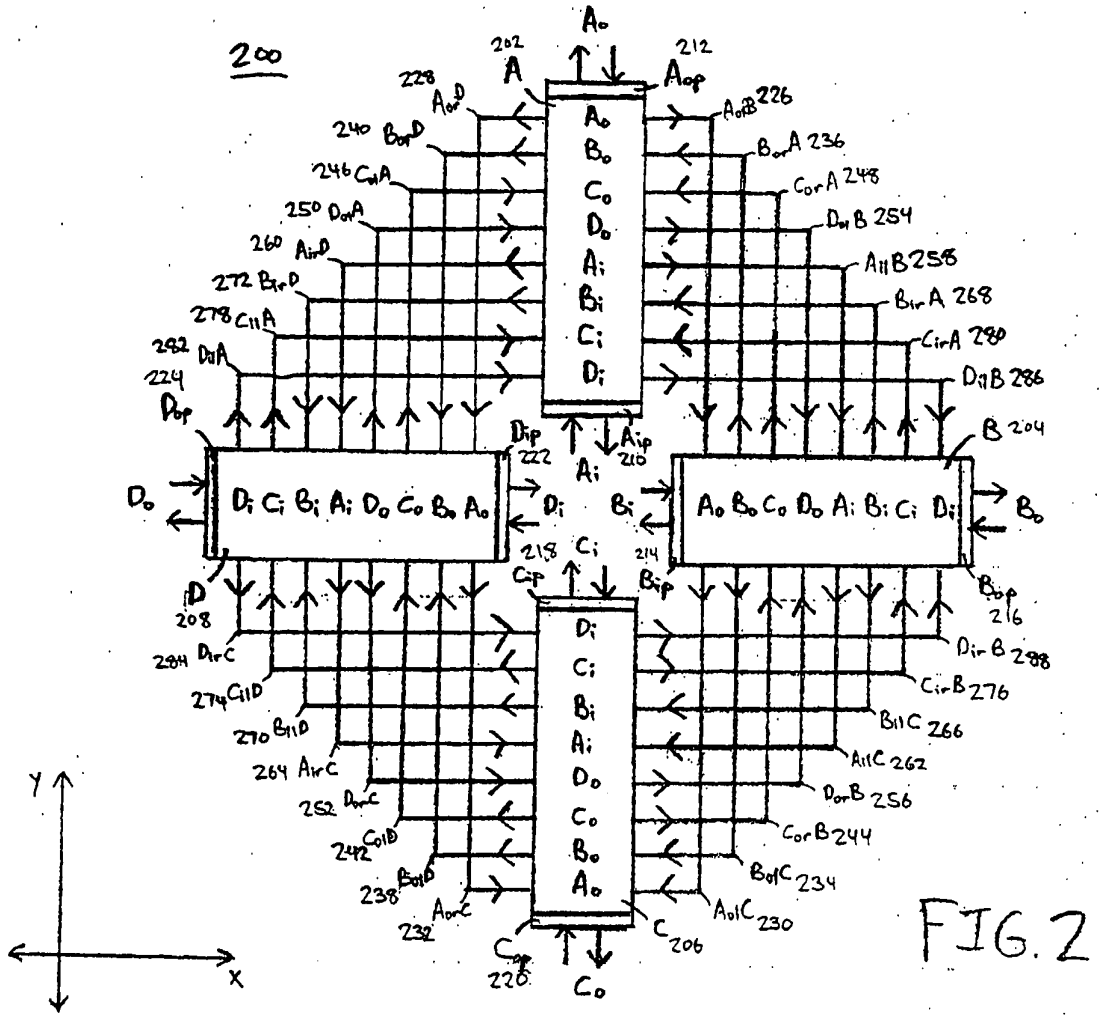

200
A
202
A_op
212
A_o
A_i
A_ip
210
B
204
B_op
216
B_o
B_i
214
C
206
C_op
220
C_o
C_i
218
D
208
D_op
224
D_o
D_i
D_ip
222
A_o B_o C_o D_o A_i B_i C_i D_i
D_i C_i B_i A_i D_o C_o B_o A_o
D_i C_i B_i A_i D_o C_o B_o A_o
A_orB 226
B_orA 236
C_orA 248
D_orB 254
A_ilB 258
B_irA 268
C_irA 280
D_ilB 286
D_irB 288
C_irB 276
B_ilC 266
A_ilC 262
D_orB 256
C_orB 244
B_olC 234
A_olC 230
A_orD 228
B_orD 240
C_olA 246
D_orA 250
A_irD 260
B_irD 272
C_ilA 278
D_ilA 282
D_irC 284
C_ilD 274
B_ilD 270
A_irC 264
D_orC 252
C_olD 242
B_olD 238
A_orC 232
Y
X

FIG. 2

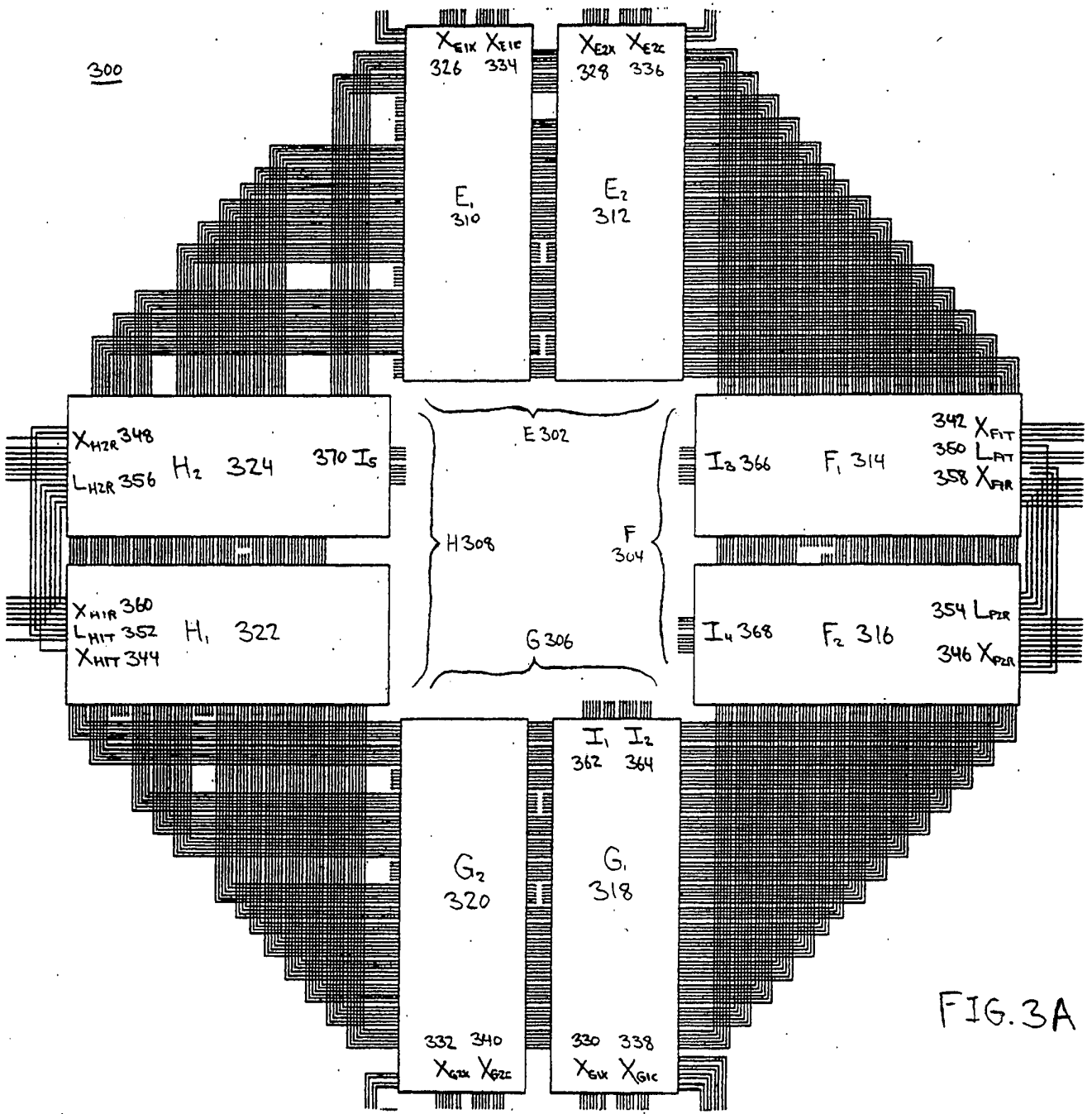

300
X_{E1X} X_{E1C}
326 334
X_{E2X} X_{E2C}
328 336
E_1
310
E_2
312
E 302
H 308
F
304
G 306
X_{H2R} 348
L_{H2R} 356
H_2 324
370 I_5
X_{H1R} 360
L_{H1T} 352
X_{H1T} 344
H_1 322
I_3 366
F_1 314
342 X_{F1T}
350 L_{F1T}
358 X_{F1R}
I_4 368
F_2 316
354 L_{F2R}
346 X_{F2R}
I_1 I_2
362 364
G_2
320
G_1
318
332 340
X_{G2X} X_{G2C}
330 338
X_{G1X} X_{G1C}

FIG. 3A

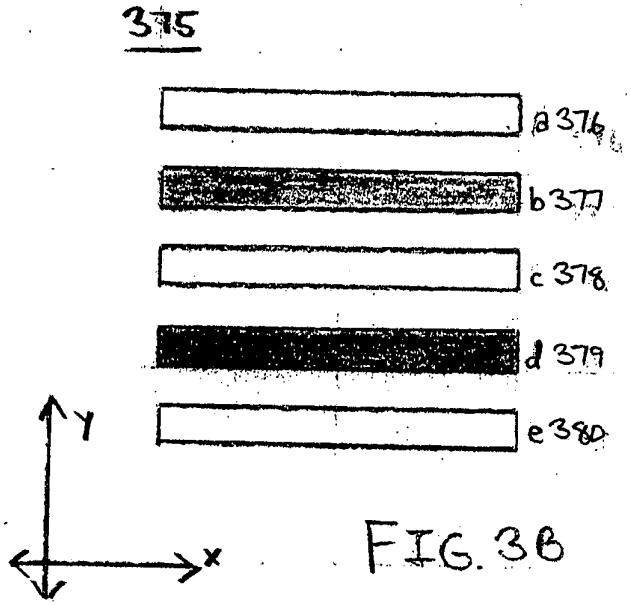

375
a 376
b 377
c 378
d 379
e 380
Y
X

FIG. 3B

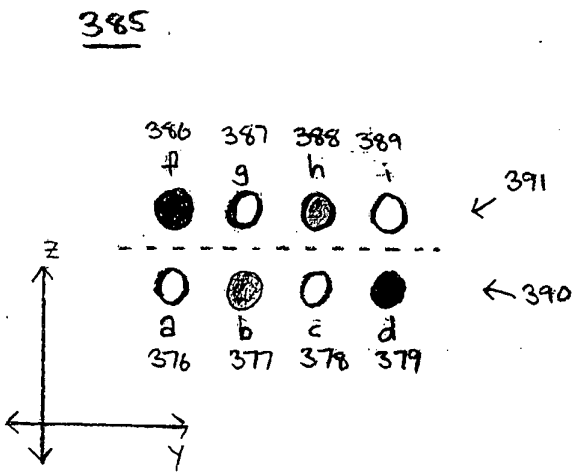

385
386 387 388 389
f g h i
391
390
a b c d
376 377 378 379
Z
Y

FIG. 3C

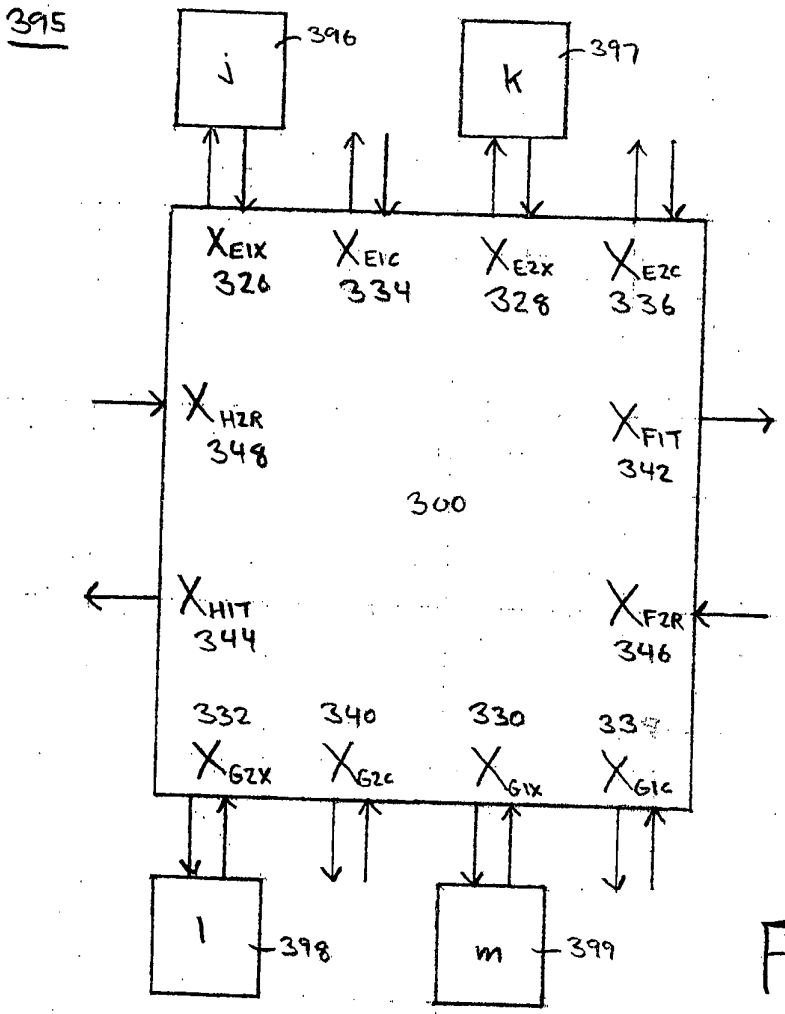

395
j
396
k
397
X_{E1X} 326
X_{E1C} 334
X_{E2X} 328
X_{E2C} 336
X_{H2R} 348
X_{FIT} 342
300
X_{HIT} 344
X_{F2R} 346
332
340
330
X_{G2X}
X_{G2C}
X_{G1X}
X_{G1C}
l
398
m
399

FIG. 3D

FIG. 4

TABLE 400

XAUI Protocol		
Received From Out of Bus	Communicated Within Bus	Transmitted to Out of Bus
40 data bits	40 data bits	80 data bits
4 link bits	4 link bits	
4 lock bits	4 lock bits	
4 clock bits	4 clock bits	4 clock bits
4 fast clock bits	4 fast clock bits	
1 CLOCK MODE SELECT bit	1 CLOCK MODE SELECT bit	

CDL Protocol		
Received From Out of Bus	Communicated Within Bus	Transmitted to Out of Bus
40 data bits	40 data bits	80 data bits
4 link bits	4 link bits	4 link bits
4 lock bits	4 lock bits	4 lock bits
4 clock bits	4 clock bits	4 clock bits
4 fast clock bits	4 fast clock bits	
1 CLOCK MODE SELECT bit	1 CLOCK MODE SELECT bit	

XGMII Protocol		
Received From Out of Bus	Communicated Within Bus	Transmitted to Out of Bus
40 data bits	80 data bits	40 data bits
4 lock bits	4 lock bits	
4 clock bits	4 clock bits	4 clock bits
3 MODE SELECT bits		
1 DIFFERENTIAL CLOCK MODE SELECT bit		
	1 CLOCK MODE SELECT bit	
		4 output enable bits

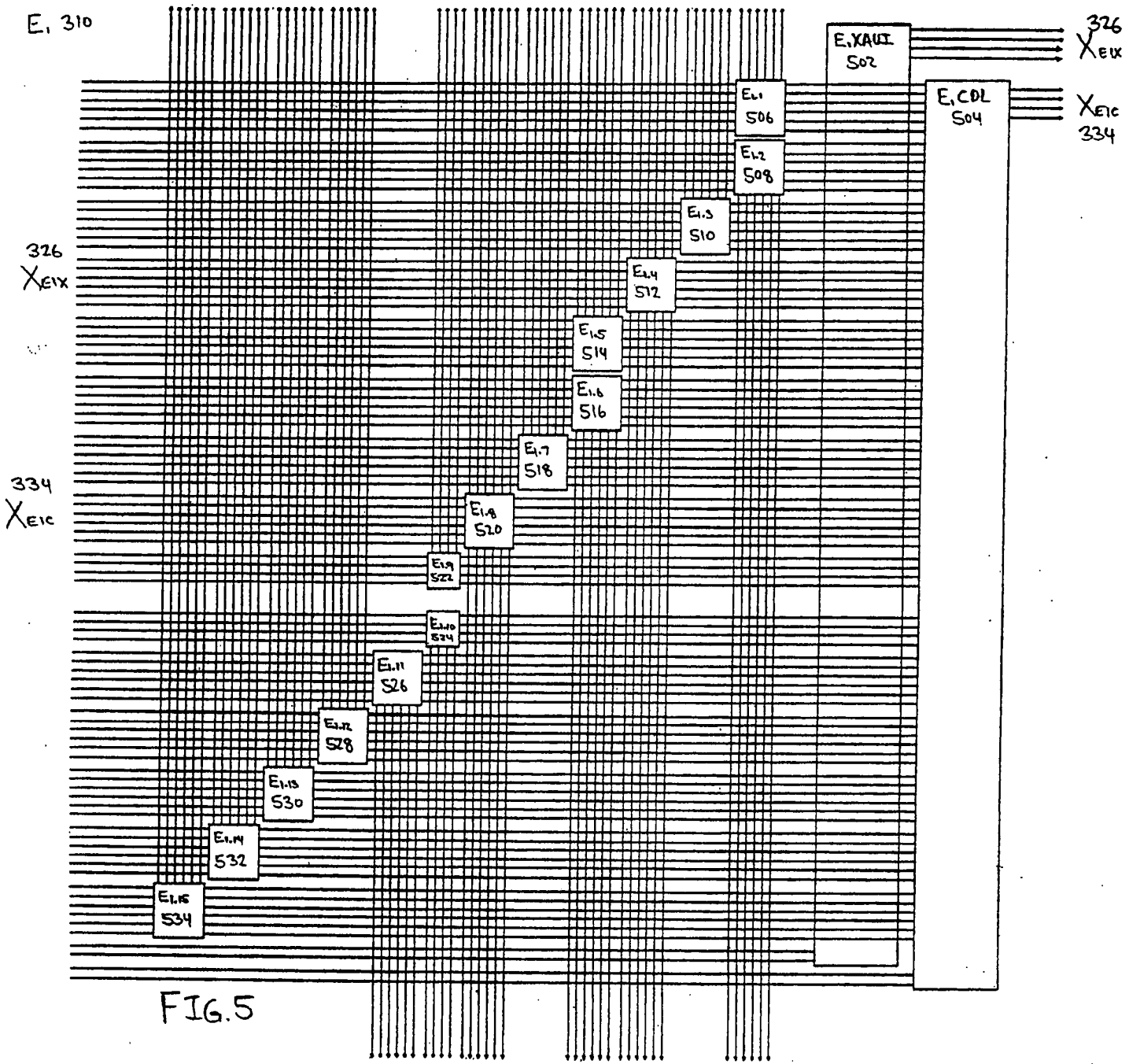

E1 310
326
XE1X
334
XE1C
E1 XAUI
502
E1 CDL
504
326
XE1X
XE1C
334
E1.1
506
E1.2
508
E1.3
510
E1.4
512
E1.5
514
E1.6
516
E1.7
518
E1.8
520
E1.9
522
E1.10
524
E1.11
526
E1.12
528
E1.13
530
E1.14
532
E1.15
534

FIG.5

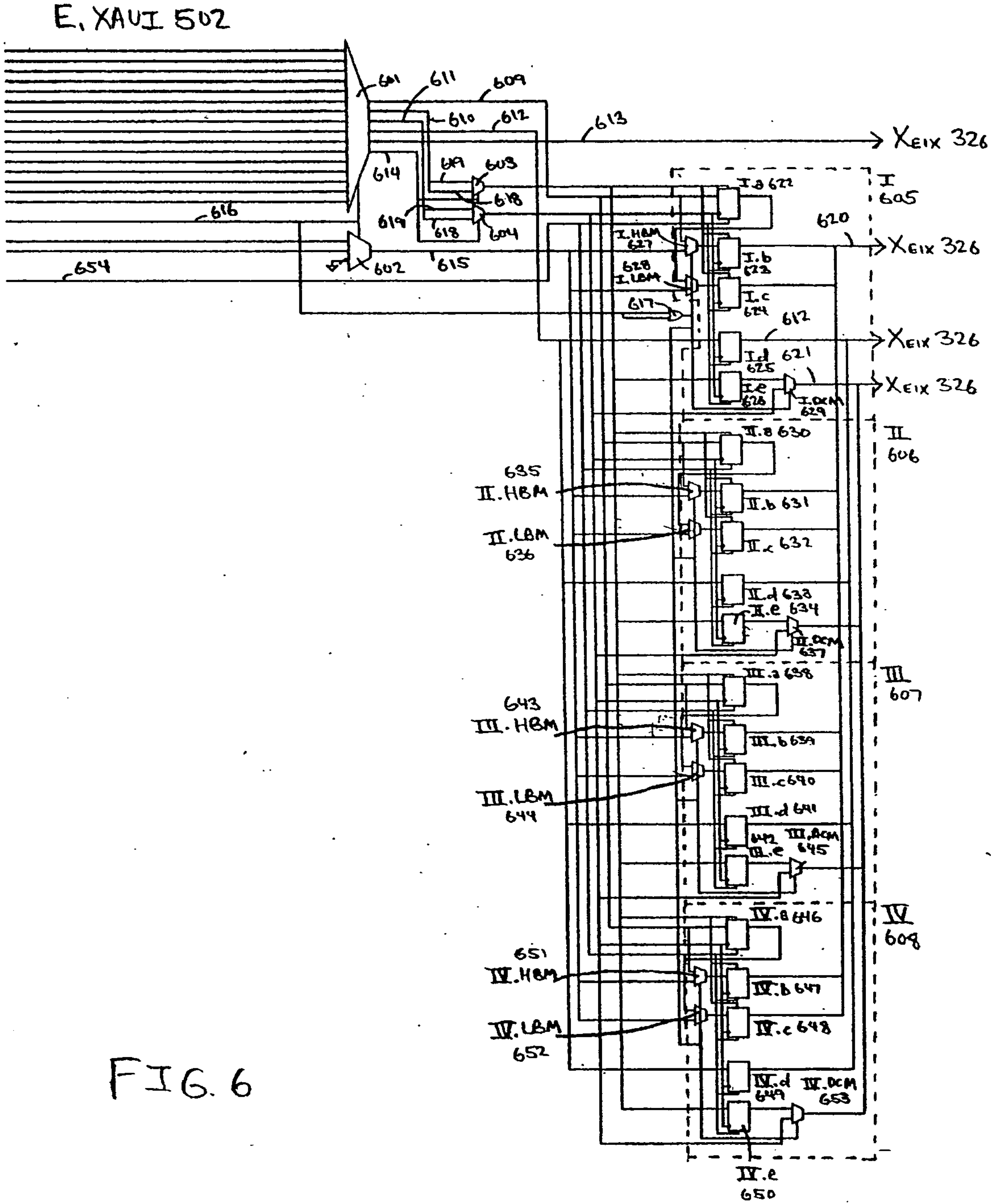

E, XAUI 502
X EIX 326
X EIX 326
X EIX 326
X EIX 326
II.HBM
II.LBM
III.HBM
III.LBM
IV.HBM
IV.LBM
IV.e
650

FIG. 6

$E_{1.1}$ 506

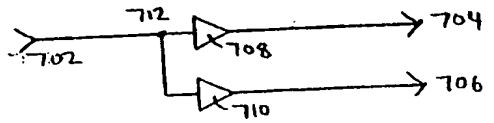


FIG. 7

$E_{1.4}$ 516

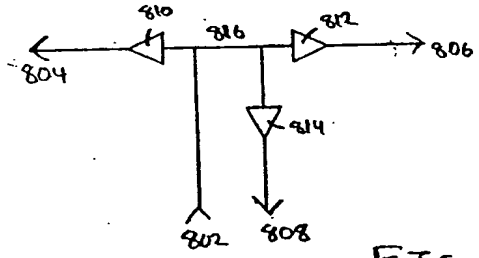


FIG. 8

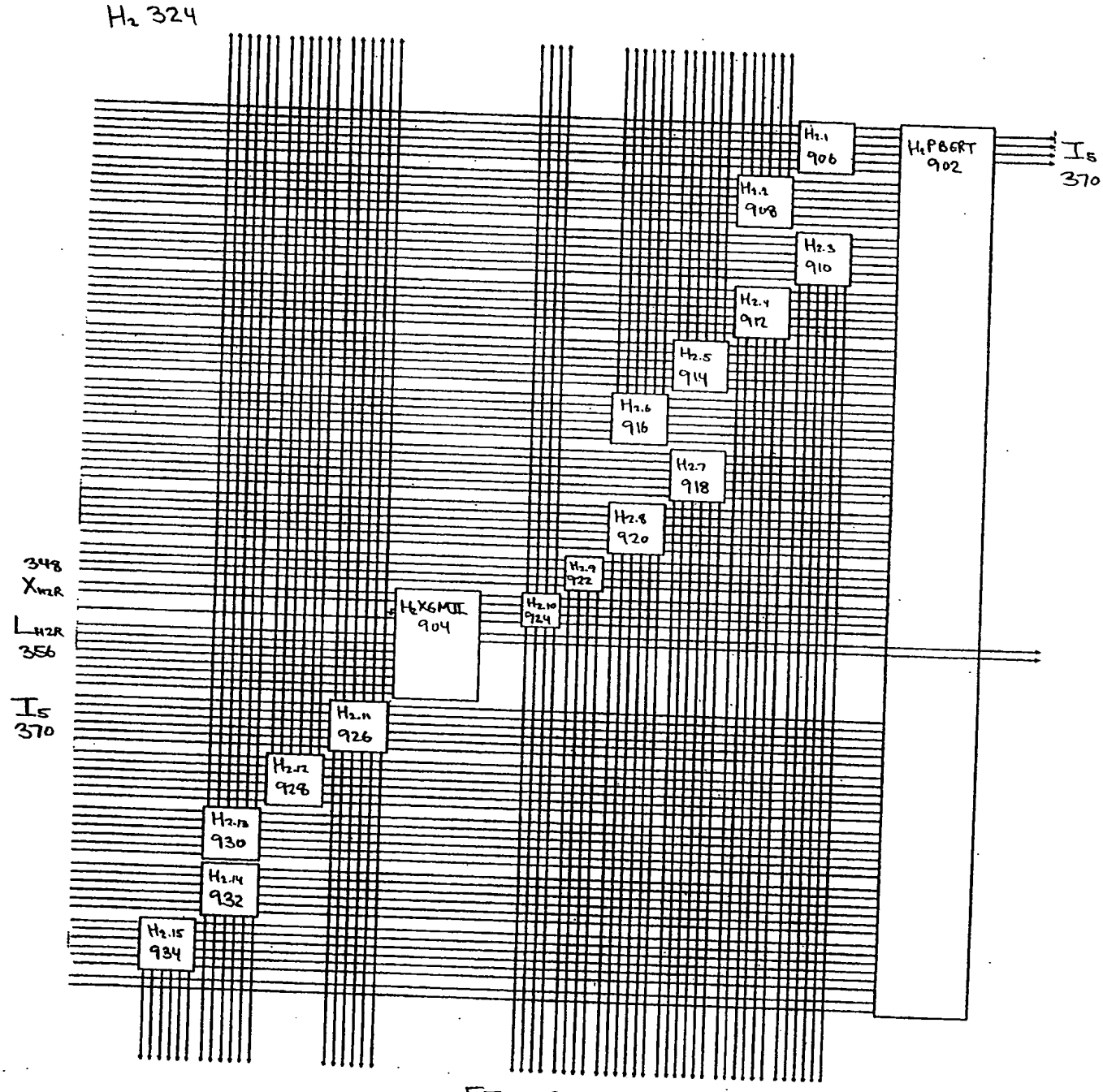

H2 324
H2.1 906
H1PBERT 902
I5 370
H2.2 908
H2.3 910
H2.4 912
H2.5 914
H2.6 916
H2.7 918
H2.8 920
H2.9 922
H2.10 924
H2XGMII 904
H2.11 926
H2.12 928
H2.13 930
H2.14 932
H2.15 934
348
XH2R
LH2R
356
I5
370

FIG. 9

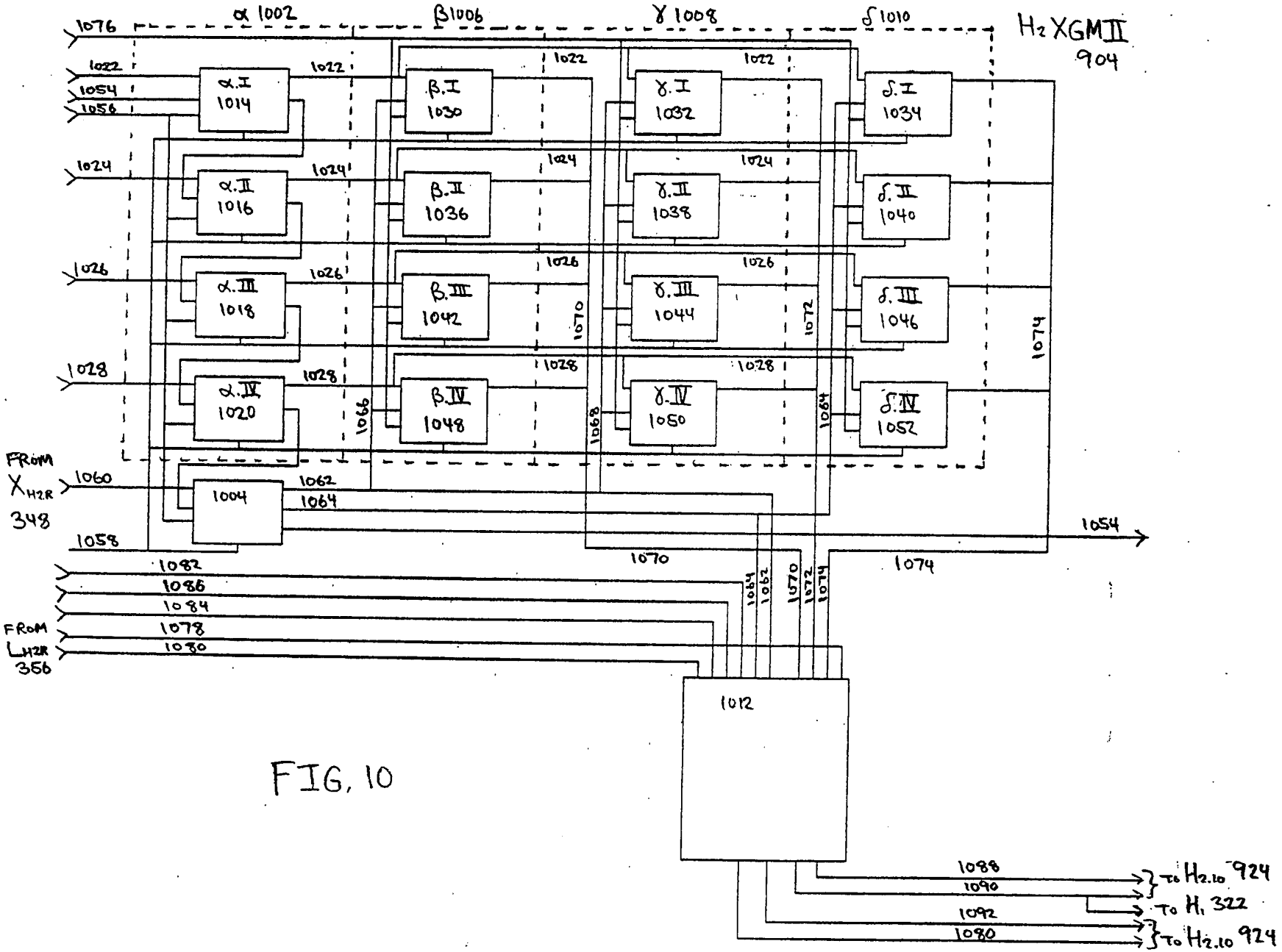

α 1002
β1006
γ 1008
δ 1010
H2XGMII
904
1076
1022
1054
1056
α.I 1014
β.I 1030
γ.I 1032
δ.I 1034
1024
α.II 1016
β.II 1036
γ.II 1038
δ.II 1040
1026
α.III 1018
β.III 1042
γ.III 1044
δ.III 1046
1028
α.IV 1020
β.IV 1048
γ.IV 1050
δ.IV 1052
1066
1068
1070
1072
1074
1004
FROM X H2R 348
1060
1062
1064
1058
1054
1082
1086
1084
1078
1080
FROM L H2R 356
1012
1088
1090
1092
1080
To H2.10 924
To H1 322
To H2.10 924

FIG. 10

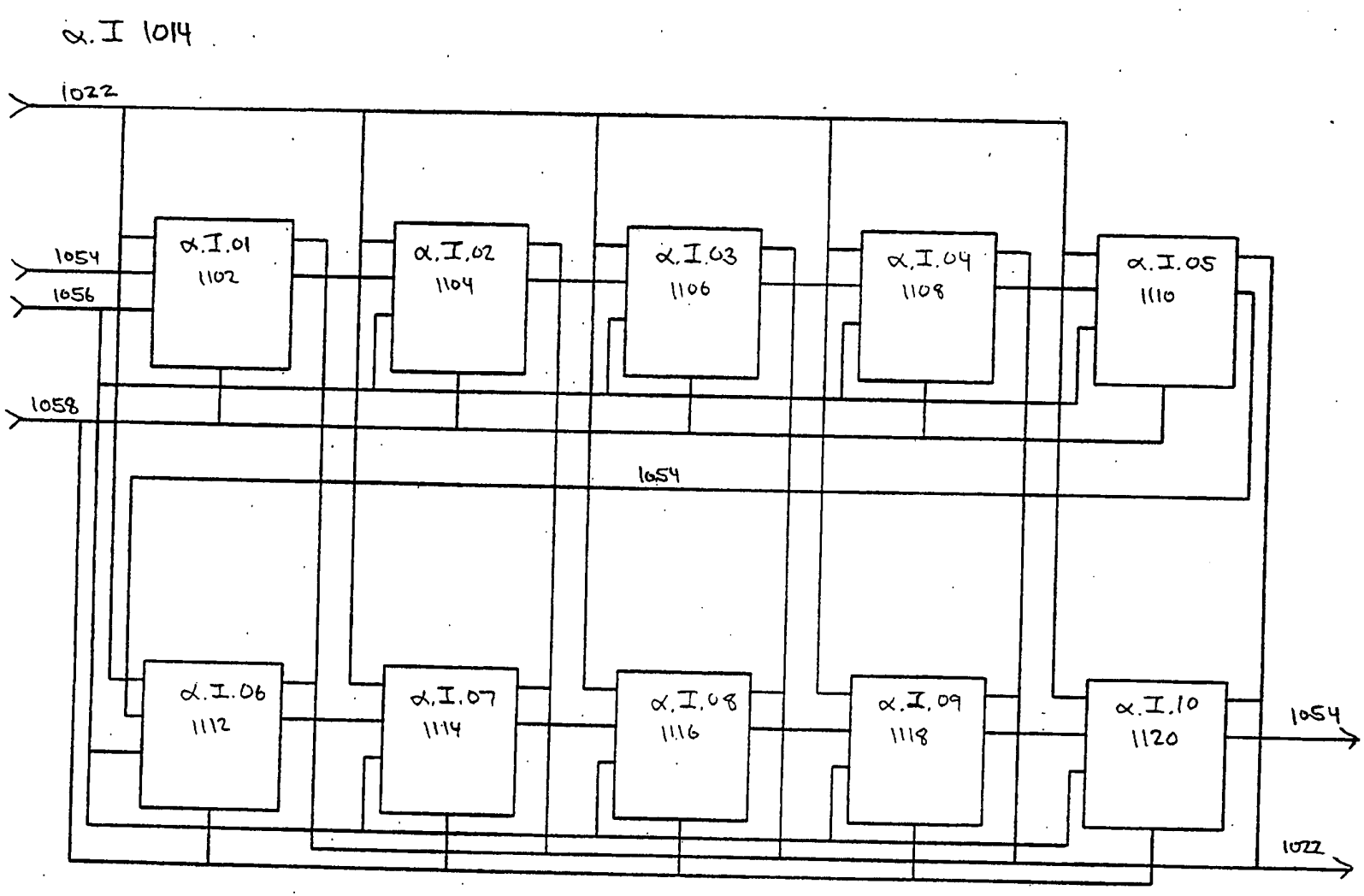

α.I 1014
1022
1054
1056
1058
α.I.01
1102
α.I.02
1104
α.I.03
1106
α.I.04
1108
α.I.05
1110
1054
α.I.06
1112
α.I.07
1114
α.I.08
1116
α.I.09
1118
α.I.10
1120
1054
1022

FIG. 11

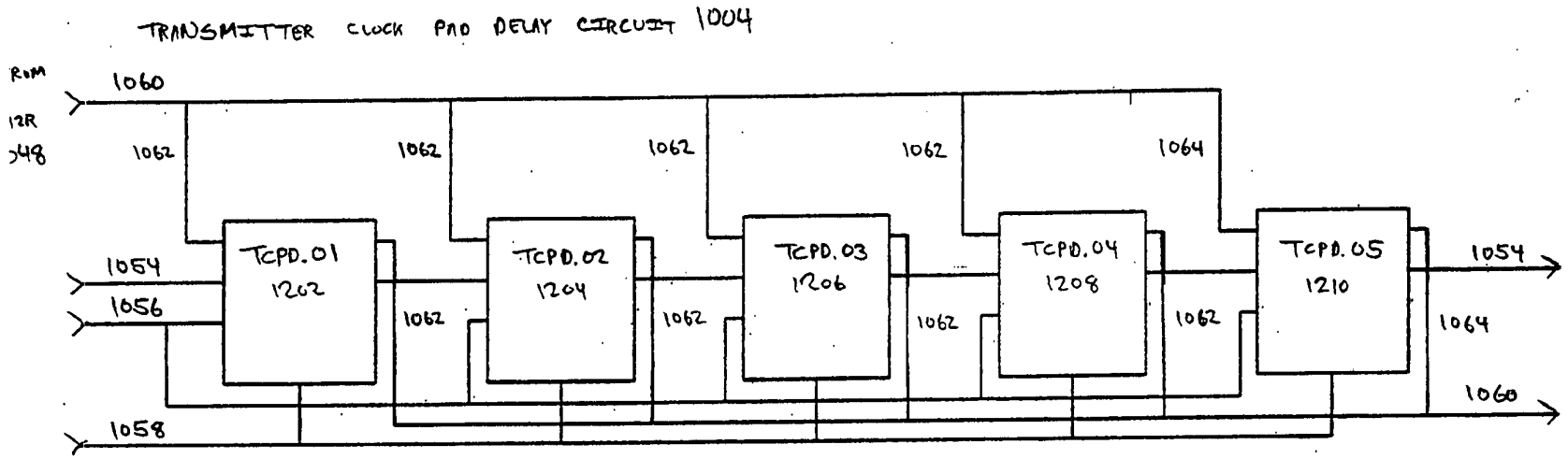

TRANSMITTER CLOCK PAD DELAY CIRCUIT 1004
RAM
12R
x48
1060
1062
1062
1062
1062
1064
1054
1056
1058
TCPD.01
1202
TCPD.02
1204
TCPD.03
1206
TCPD.04
1208
TCPD.05
1210
1062
1062
1062
1062
1054
1064
1060

FIG. 12

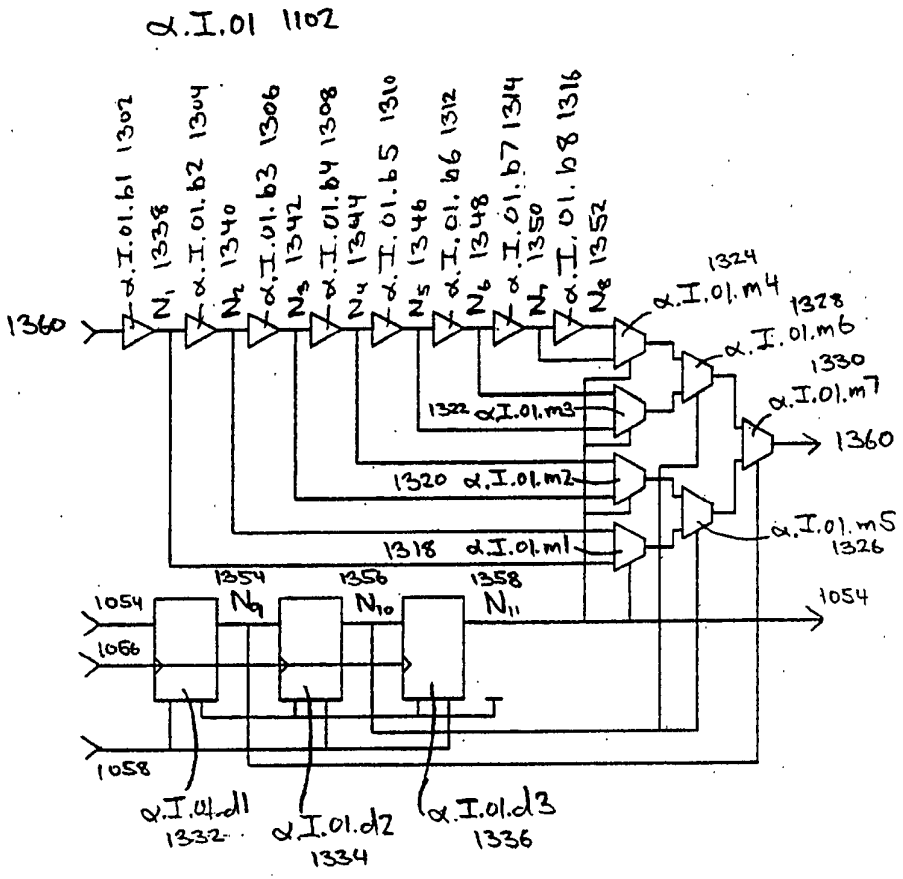


FIG. 13A

FIG. 13B
1380

N_9	N_{10}	N_{11}	Output
0	0	0	N_1
0	0	1	N_2
0	1	0	N_3
0	1	1	N_4
1	0	0	N_5
1	0	1	N_6
1	1	0	N_7
1	1	1	N_8

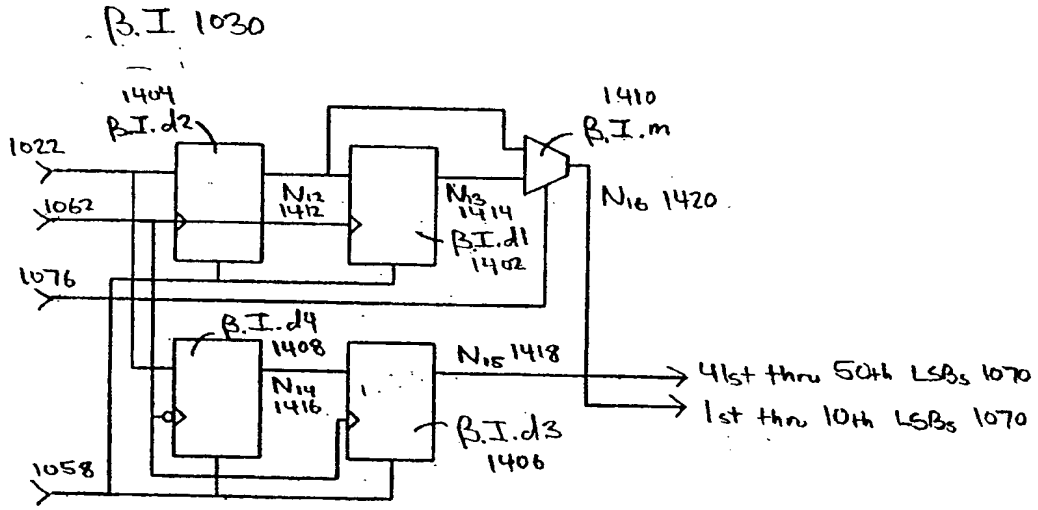
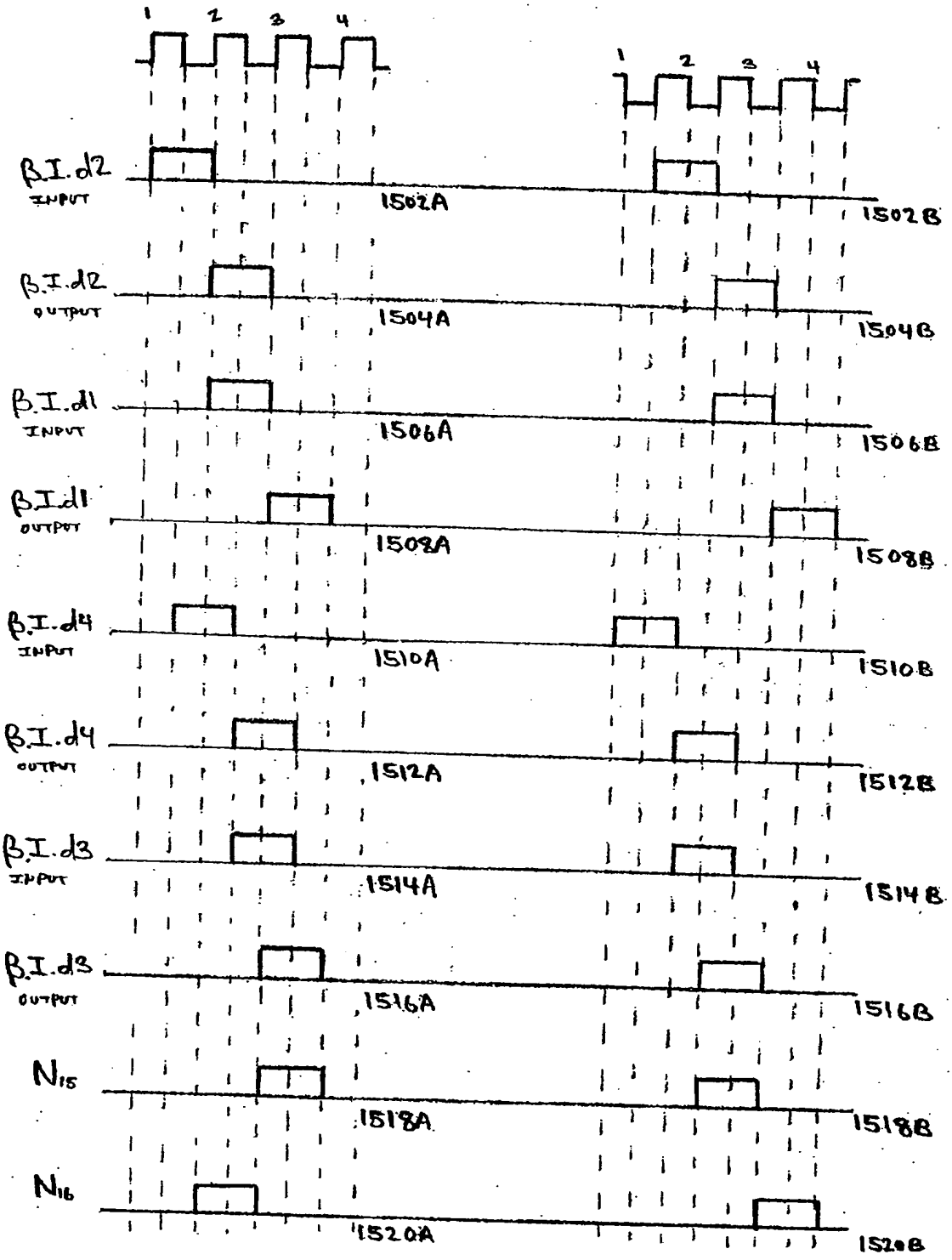

B.I 1030
1404
B.I.d2
1410
B.I.m
1022
1062
1076
1058
N12 1412
N13 1414
B.I.d1 1402
N16 1420
B.I.d4 1408
N14 1416
N15 1418
B.I.d3 1406
41st thru 50th LSBs 1070
1st thru 10th LSBs 1070

FIG. 14

FIG. 15A
1500A

FIG. 15B
1500B



TRANSMITTER REGISTER MULTIPLEXER 1012

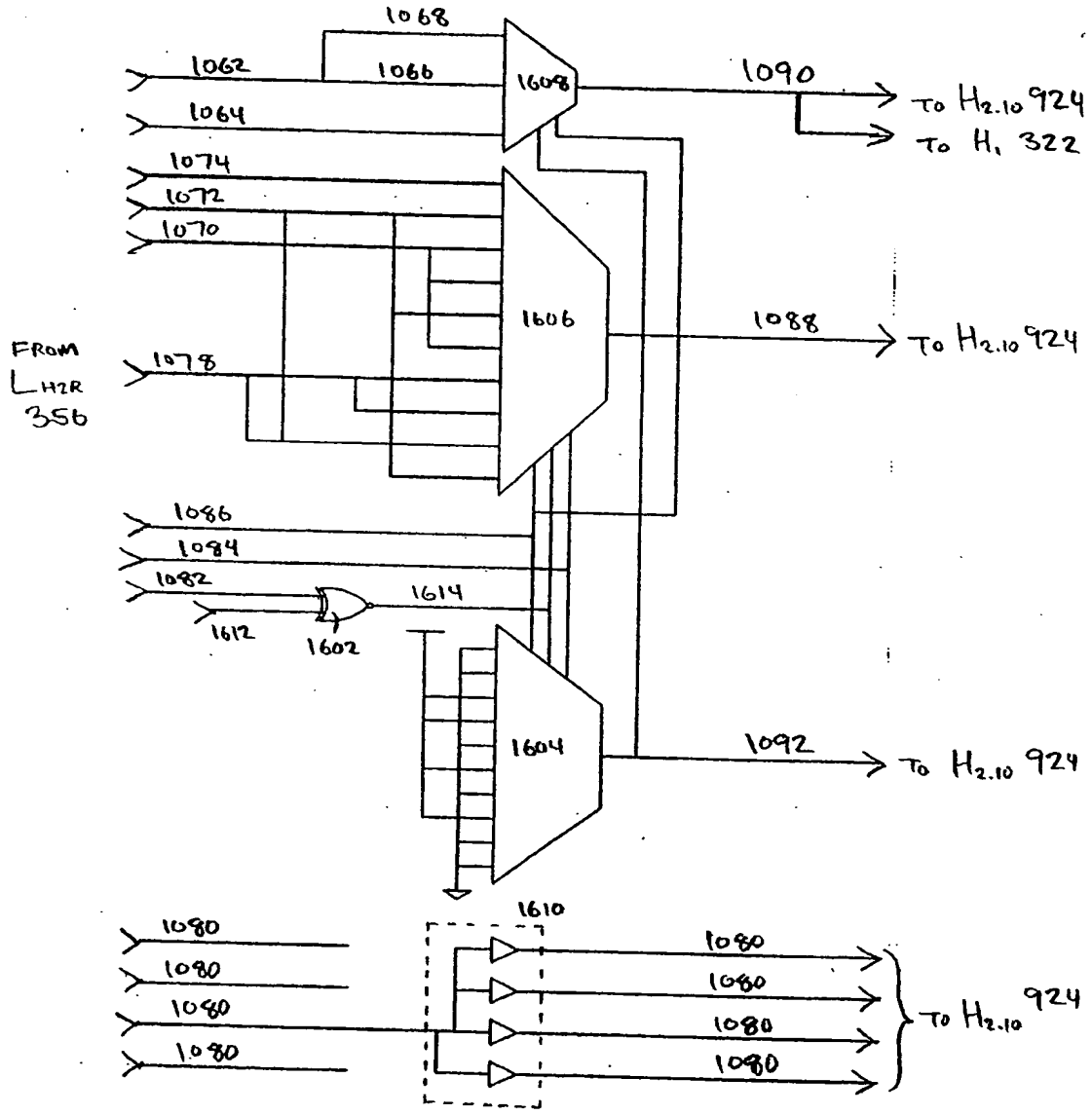


FIG. 16

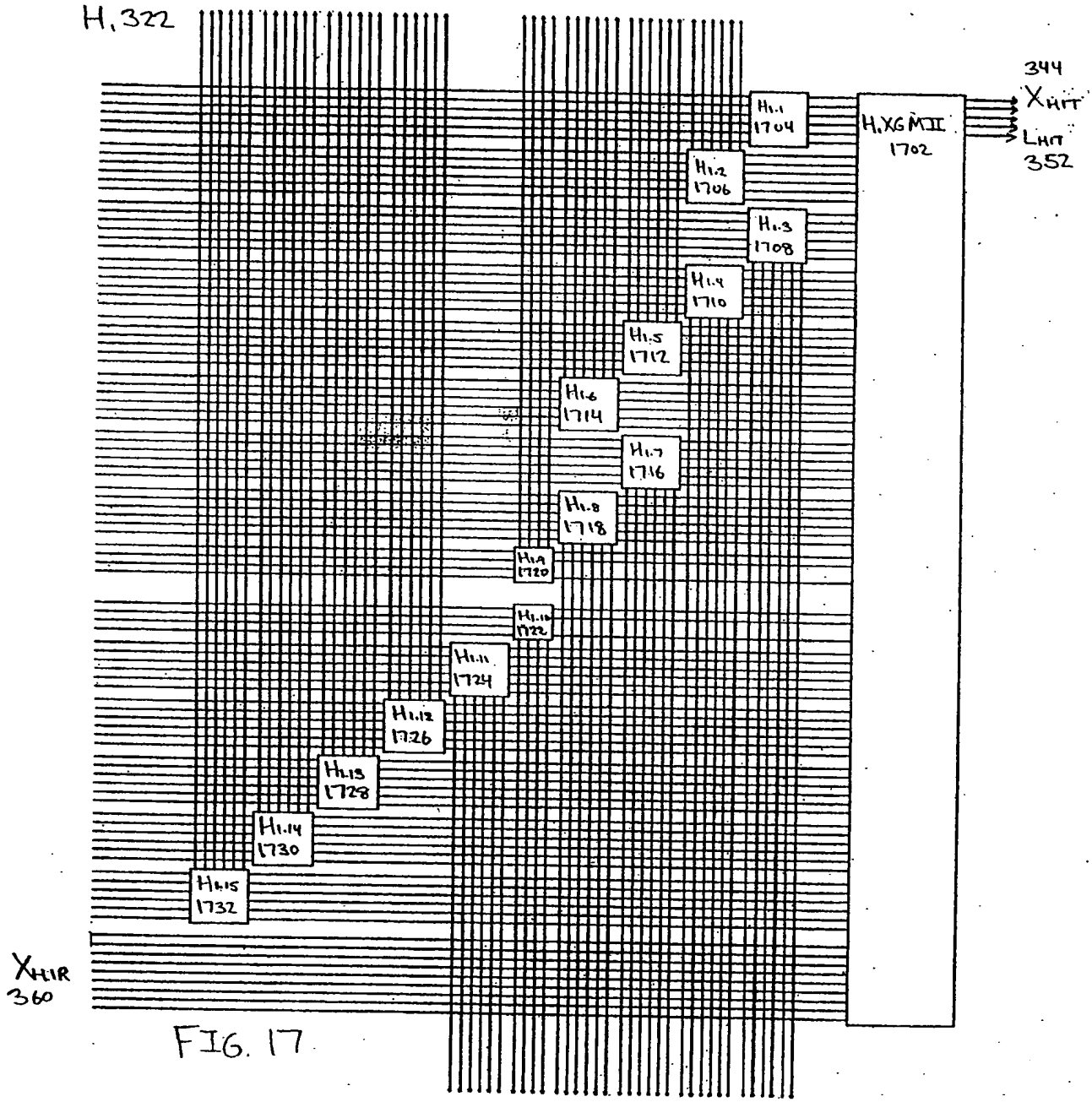

H.322
344
XHIT
LHIT
352
H.XGMII
1702
H.1
1704
H.2
1706
H.3
1708
H.4
1710
H.5
1712
H.6
1714
H.7
1716
H.8
1718
H.9
1720
H.10
1722
H.11
1724
H.12
1726
H.13
1728
H.14
1730
H.15
1732
XHIR
360

FIG. 17

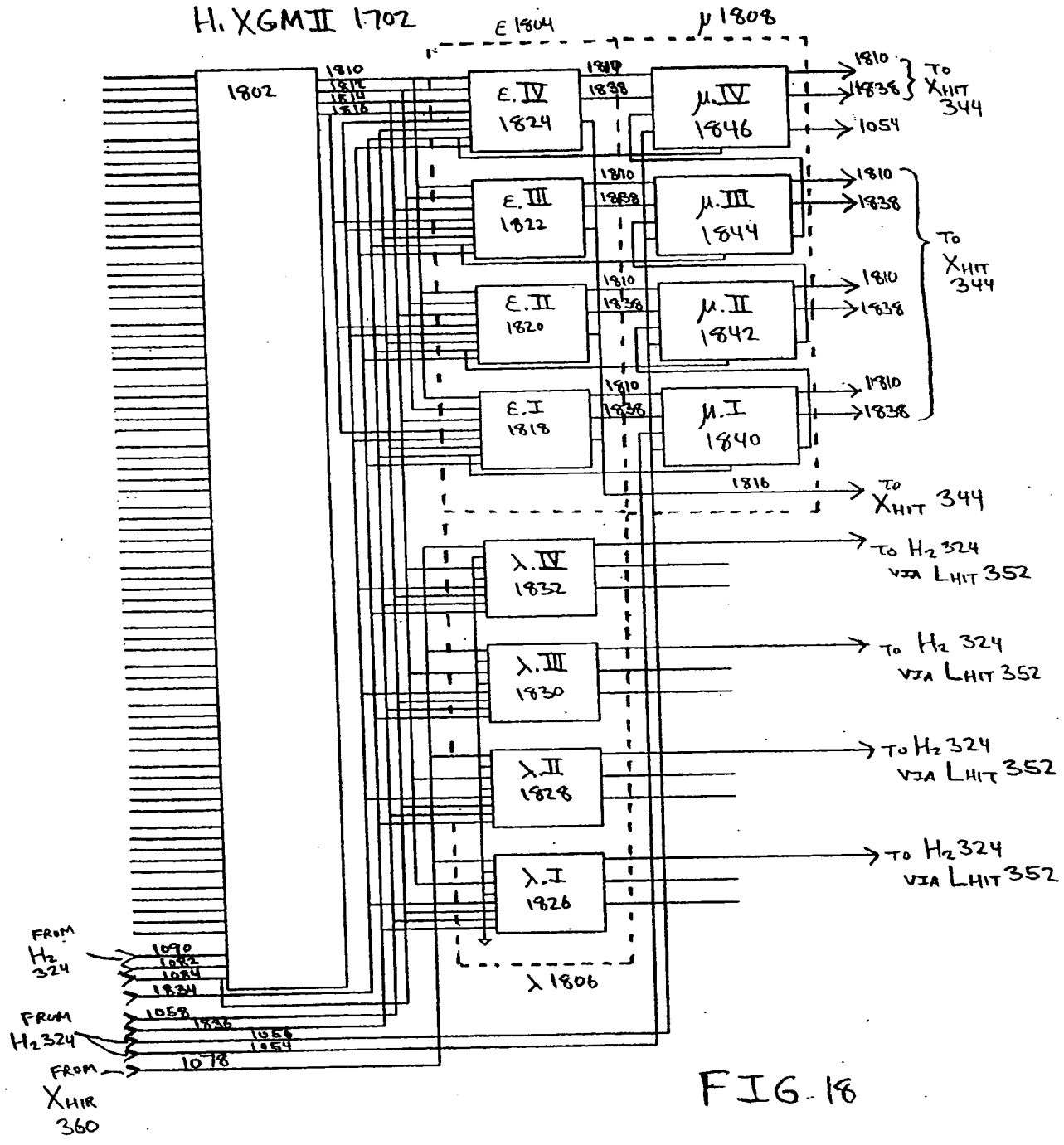

H. XGM II 1702
ε 1804
μ 1808
1802
ε.IV 1824
ε.III 1822
ε.II 1820
ε.I 1818
μ.IV 1846
μ.III 1844
μ.II 1842
μ.I 1840
λ.IV 1832
λ.III 1830
λ.II 1828
λ.I 1826
λ 1806
1810
1838
1816
1054
To X HIT 344
To H2 324 VIA L HIT 352
FROM H2 324
FROM X HIR 360
1090
1092
1094
1834
1058
1836
1056
1054
1078

FIG. 18

RECEIVER AND MULTIPLEXER 1802

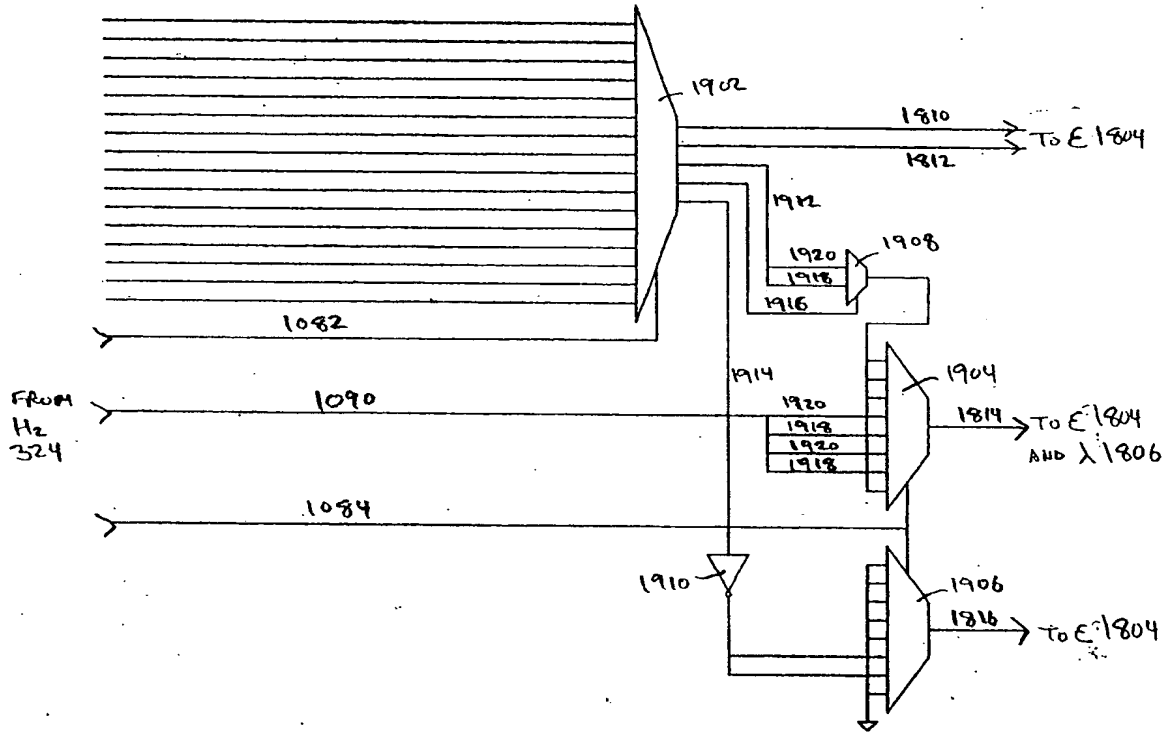


FIG. 19

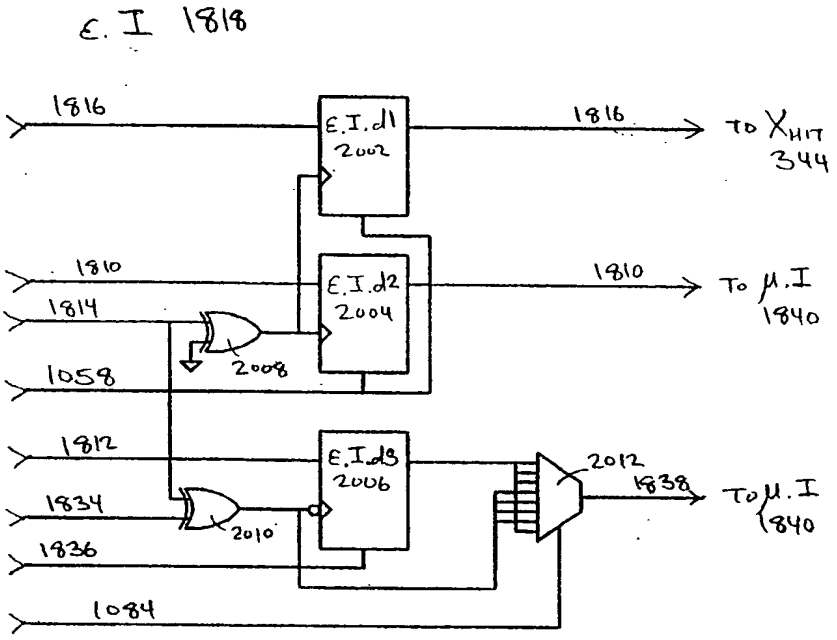

E.I 1818
1816
E.I.d1
2002
1816
To X_HIT
344
1810
E.I.d2
2004
1810
To μ.I
1840
1814
2008
1058
1812
E.I.d3
2006
2012
1838
To μ.I
1840
1834
2010
1836
1084

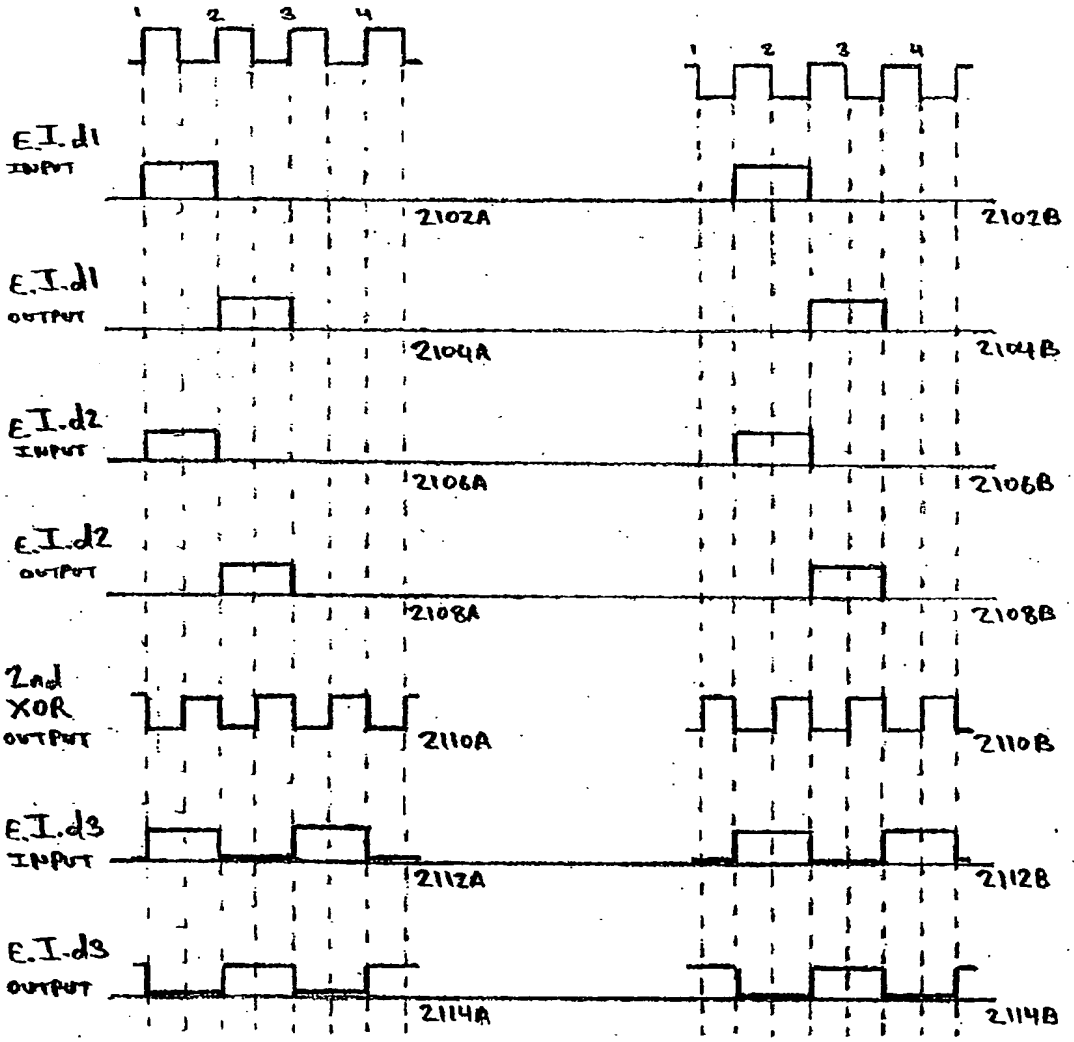
FIG. 20

FIG. 21A

2100A

FIG. 21B

2100B



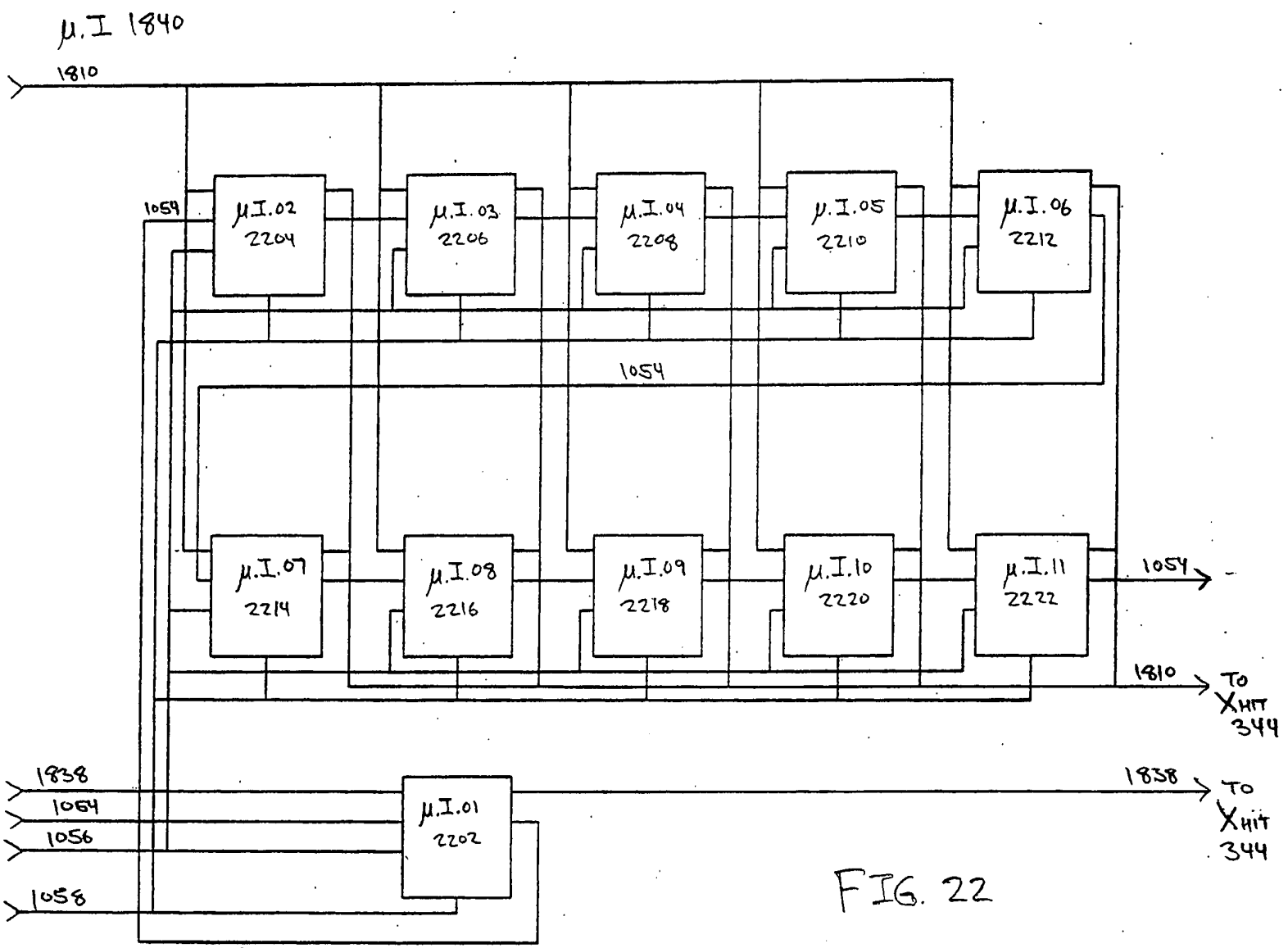

μ.I 1840
1810
1059
μ.I.02
2204
μ.I.03
2206
μ.I.04
2208
μ.I.05
2210
μ.I.06
2212
1054
μ.I.07
2214
μ.I.08
2216
μ.I.09
2218
μ.I.10
2220
μ.I.11
2222
1054
1810
TO
XHIT
344
1838
1064
1056
1058
μ.I.01
2202
1838
TO
XHIT
344

FIG. 22

FIG. 23

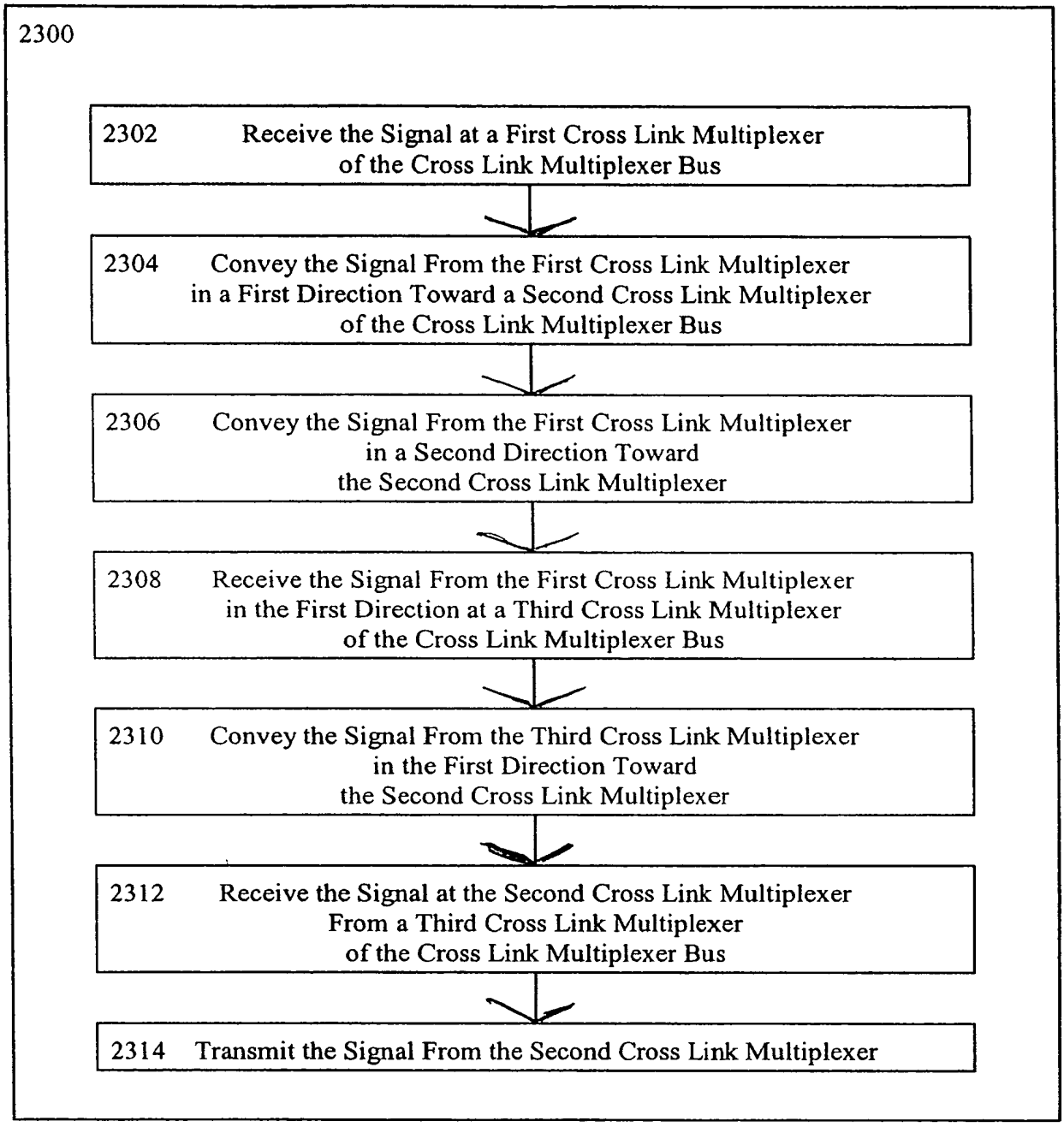

2300
2302 Receive the Signal at a First Cross Link Multiplexer of the Cross Link Multiplexer Bus
2304 Convey the Signal From the First Cross Link Multiplexer in a First Direction Toward a Second Cross Link Multiplexer of the Cross Link Multiplexer Bus
2306 Convey the Signal From the First Cross Link Multiplexer in a Second Direction Toward the Second Cross Link Multiplexer
2308 Receive the Signal From the First Cross Link Multiplexer in the First Direction at a Third Cross Link Multiplexer of the Cross Link Multiplexer Bus
2310 Convey the Signal From the Third Cross Link Multiplexer in the First Direction Toward the Second Cross Link Multiplexer
2312 Receive the Signal at the Second Cross Link Multiplexer From a Third Cross Link Multiplexer of the Cross Link Multiplexer Bus
2314 Transmit the Signal From the Second Cross Link Multiplexer

FIG. 24

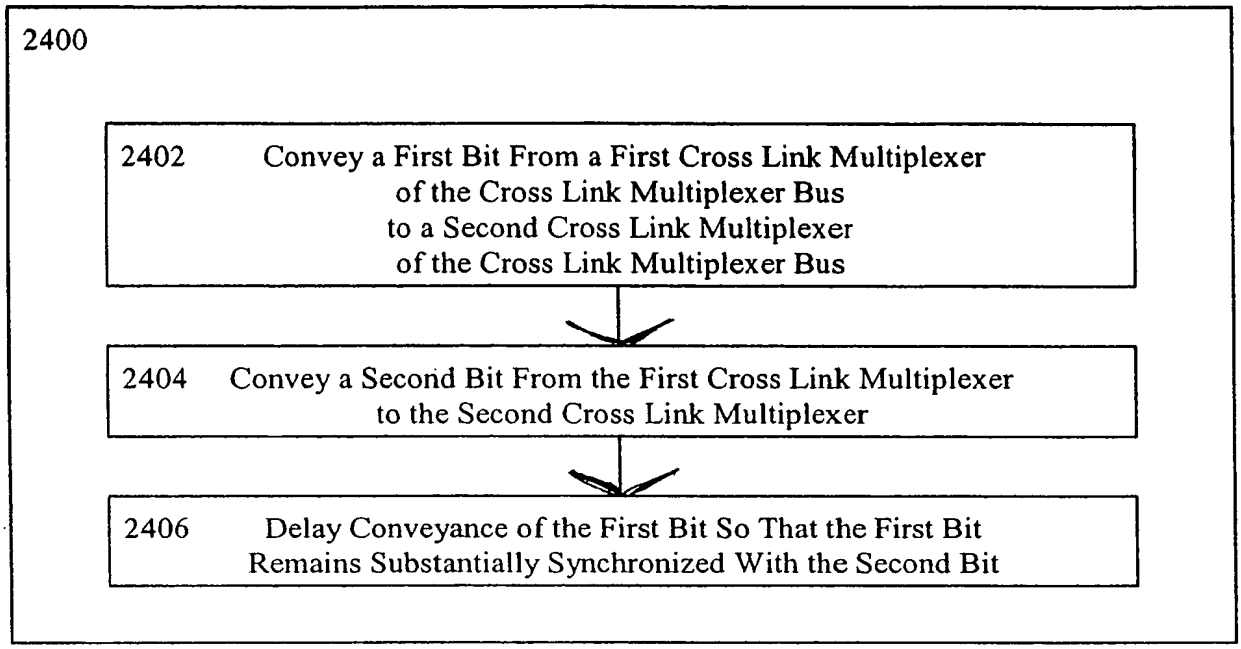

2400
2402 Convey a First Bit From a First Cross Link Multiplexer of the Cross Link Multiplexer Bus to a Second Cross Link Multiplexer of the Cross Link Multiplexer Bus
2404 Convey a Second Bit From the First Cross Link Multiplexer to the Second Cross Link Multiplexer
2406 Delay Conveyance of the First Bit So That the First Bit Remains Substantially Synchronized With the Second Bit

FIG. 25

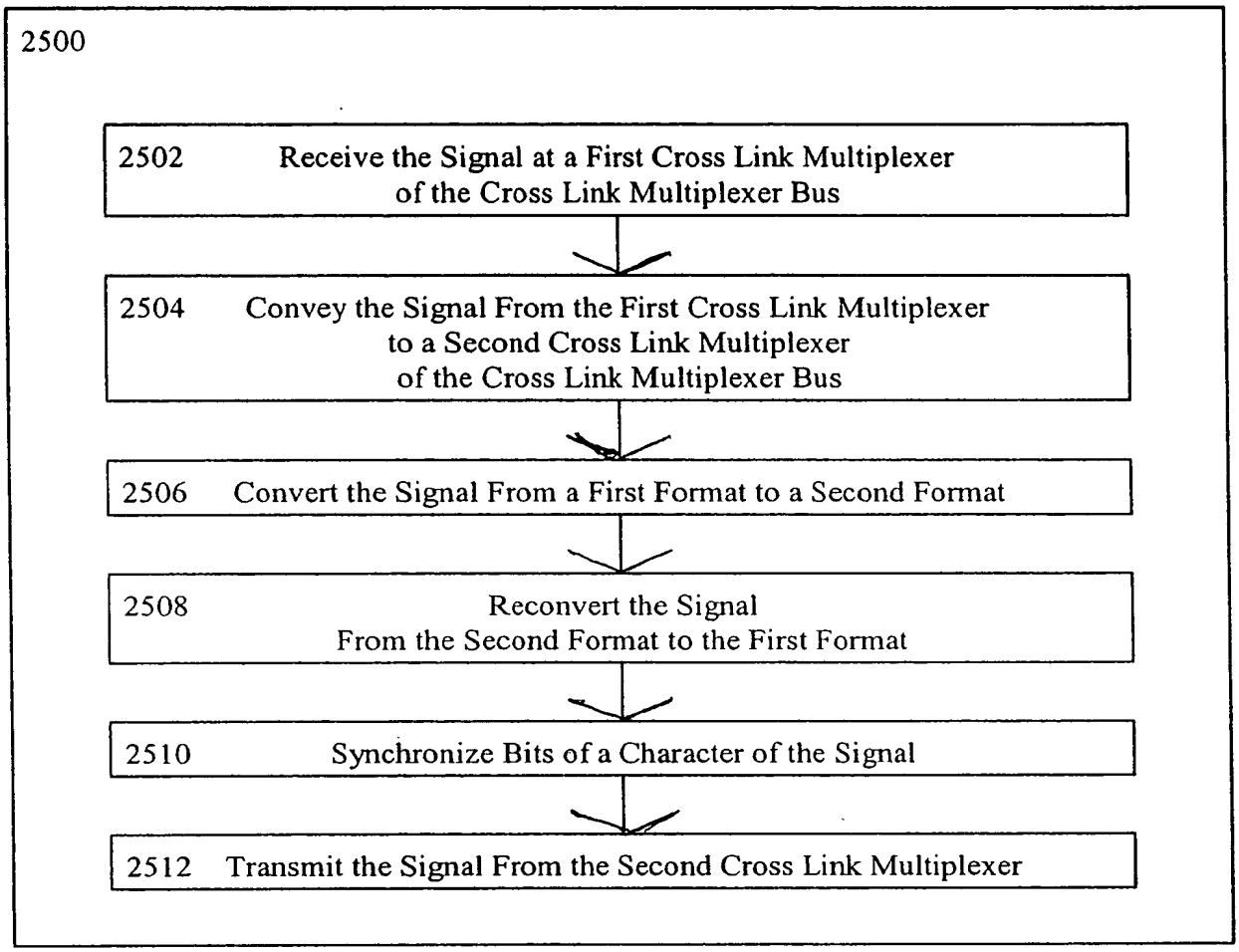

2500
2502 Receive the Signal at a First Cross Link Multiplexer of the Cross Link Multiplexer Bus
2504 Convey the Signal From the First Cross Link Multiplexer to a Second Cross Link Multiplexer of the Cross Link Multiplexer Bus
2506 Convert the Signal From a First Format to a Second Format
2508 Reconvert the Signal From the Second Format to the First Format
2510 Synchronize Bits of a Character of the Signal
2512 Transmit the Signal From the Second Cross Link Multiplexer

FIG. 26

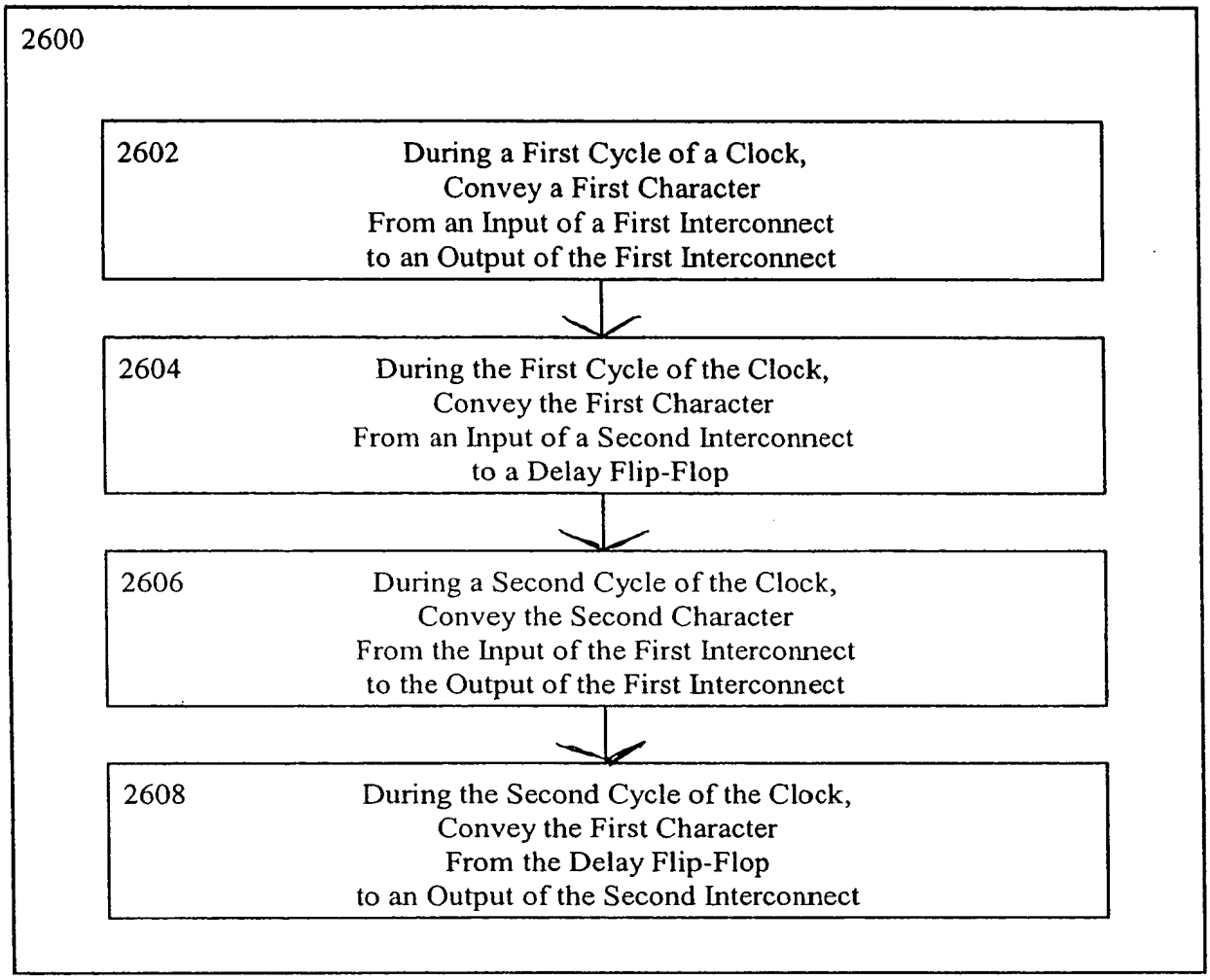

2600
2602
During a First Cycle of a Clock,
Convey a First Character
From an Input of a First Interconnect
to an Output of the First Interconnect
2604
During the First Cycle of the Clock,
Convey the First Character
From an Input of a Second Interconnect
to a Delay Flip-Flop
2606
During a Second Cycle of the Clock,
Convey the Second Character
From the Input of the First Interconnect
to the Output of the First Interconnect
2608
During the Second Cycle of the Clock,
Convey the First Character
From the Delay Flip-Flop
to an Output of the Second Interconnect

FIG. 27

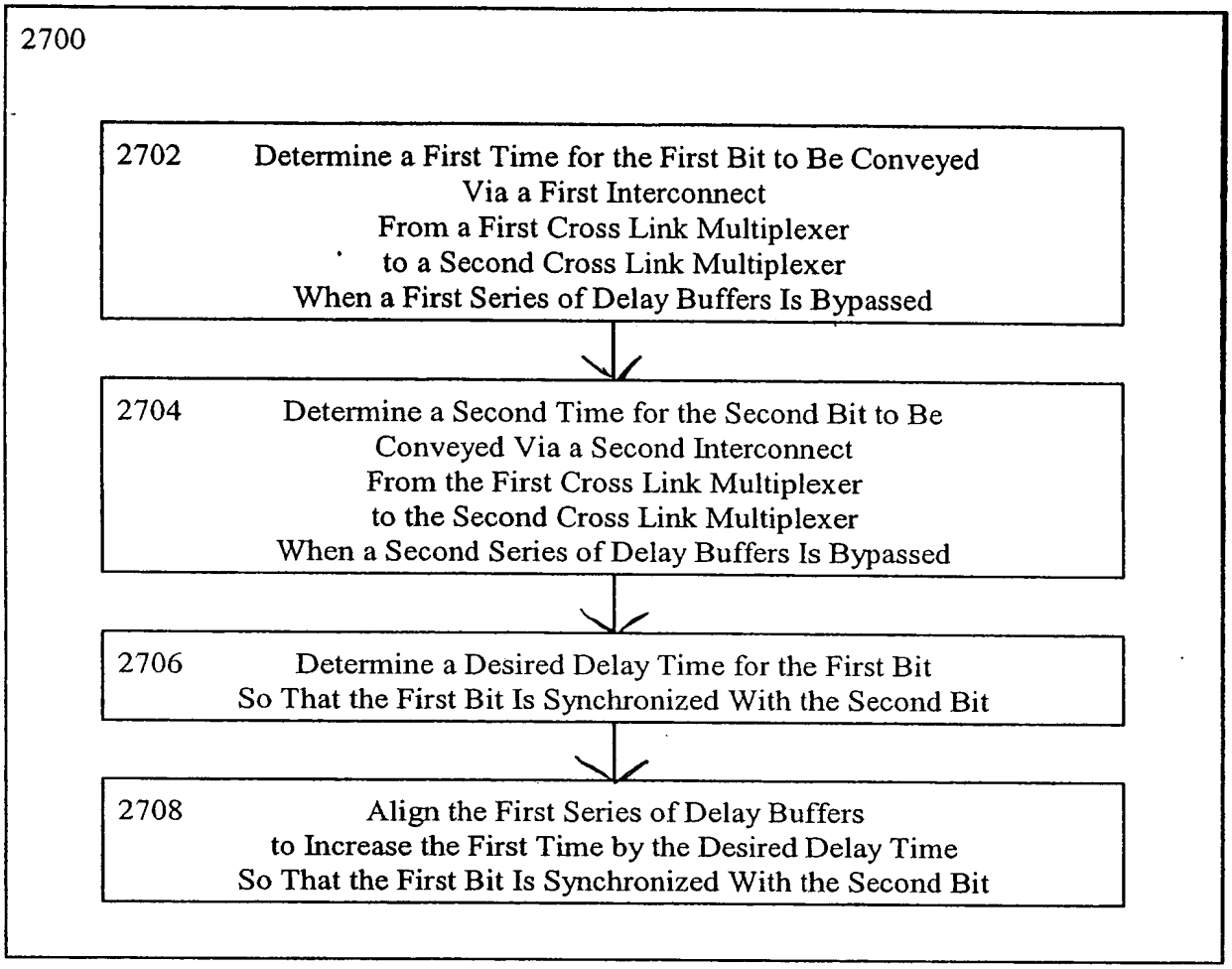

2700
2702
Determine a First Time for the First Bit to Be Conveyed
Via a First Interconnect
From a First Cross Link Multiplexer
to a Second Cross Link Multiplexer
When a First Series of Delay Buffers Is Bypassed
2704
Determine a Second Time for the Second Bit to Be
Conveyed Via a Second Interconnect
From the First Cross Link Multiplexer
to the Second Cross Link Multiplexer
When a Second Series of Delay Buffers Is Bypassed
2706
Determine a Desired Delay Time for the First Bit
So That the First Bit Is Synchronized With the Second Bit
2708
Align the First Series of Delay Buffers
to Increase the First Time by the Desired Delay Time
So That the First Bit Is Synchronized With the Second Bit

FIG. 28

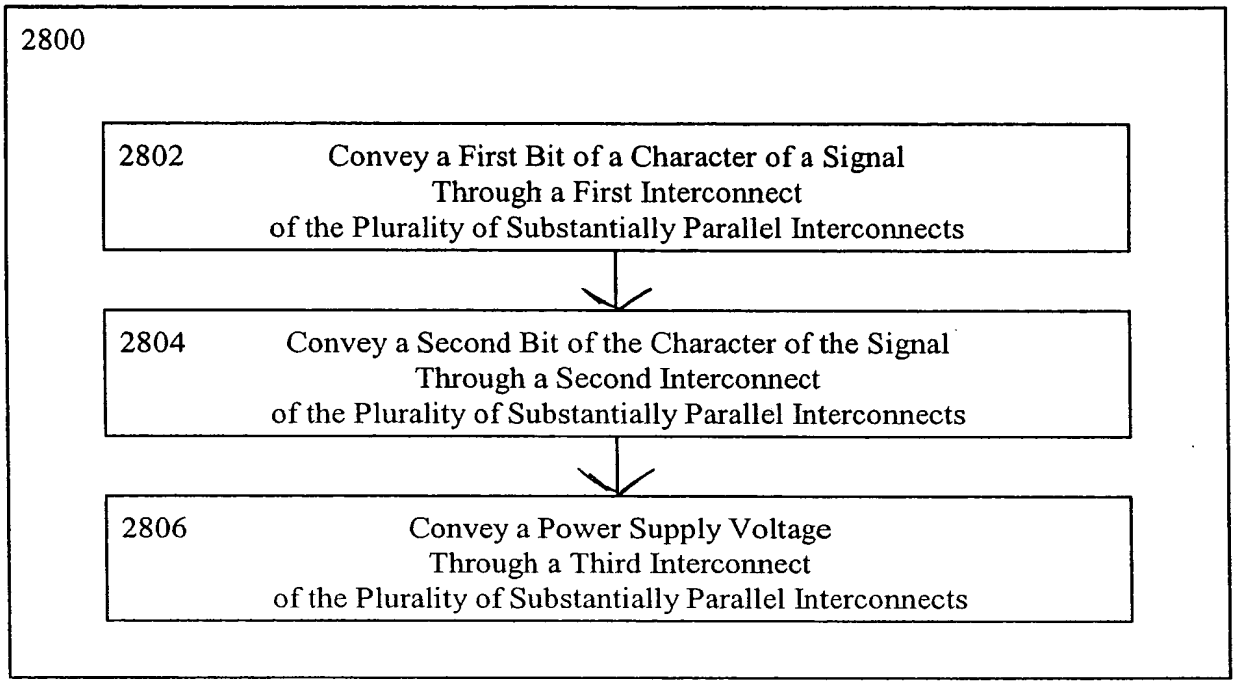
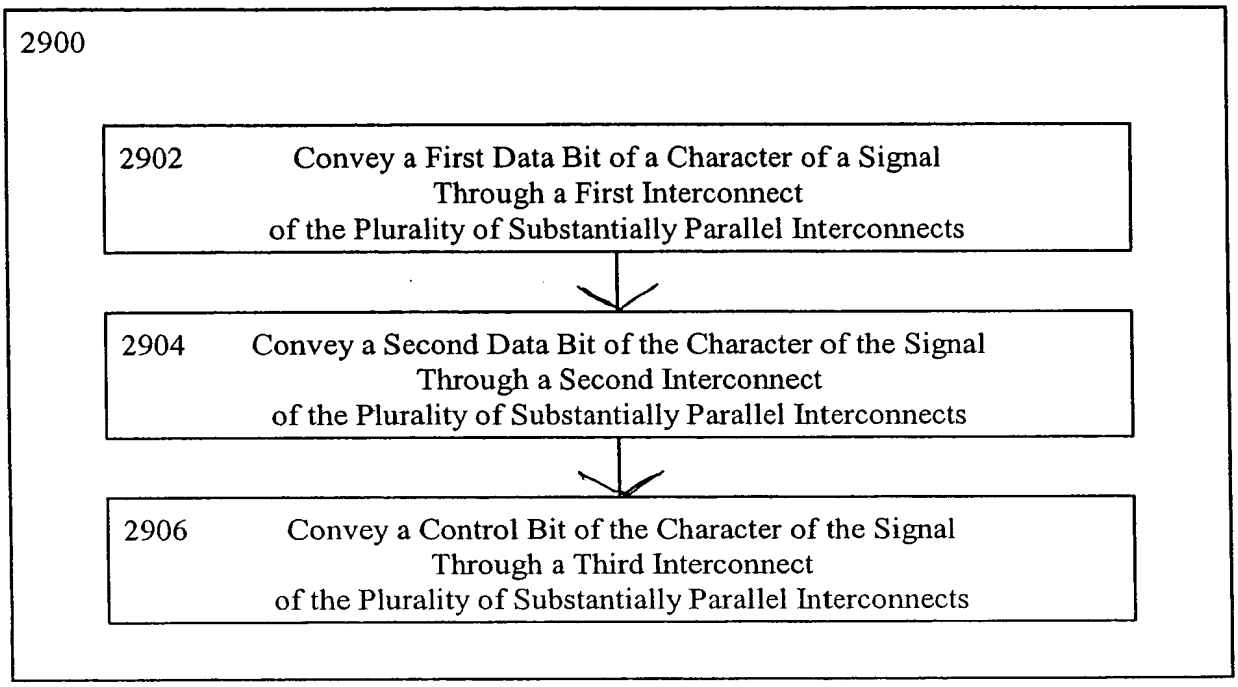

2800
2802
Convey a First Bit of a Character of a Signal
Through a First Interconnect
of the Plurality of Substantially Parallel Interconnects
2804
Convey a Second Bit of the Character of the Signal
Through a Second Interconnect
of the Plurality of Substantially Parallel Interconnects
2806
Convey a Power Supply Voltage
Through a Third Interconnect
of the Plurality of Substantially Parallel Interconnects

FIG. 29


2900
2902
Convey a First Data Bit of a Character of a Signal
Through a First Interconnect
of the Plurality of Substantially Parallel Interconnects
2904
Convey a Second Data Bit of the Character of the Signal
Through a Second Interconnect
of the Plurality of Substantially Parallel Interconnects
2906
Convey a Control Bit of the Character of the Signal
Through a Third Interconnect
of the Plurality of Substantially Parallel Interconnects